WHAT IS CLAIMED IS:

1. A method of operating a multibit delta-sigma modulator, comprising the steps of:

generating a plurality of integrator outputs from an input signal;

calculating a sum whose inputs are selected from the integrator outputs and the input signal; and

deriving a quantized value from the sum, said deriving step including the step of selectively enabling an additional quantizer level during a ramp up sequence of the modulator.

2. The method of Claim 1, further comprising the step of feeding the quantized value to an input of a pulse width modulation encoder.

3. The method of Claim 1, wherein the additional quantizer level is disabled during normal operation of the modulator.

4. The method of Claim 1, wherein said deriving step includes the step of truncating the sum.

5. The method of Claim 4, wherein said deriving step further includes the step of clipping a truncated sum within a first range of quantizer levels during the ramp up sequence and within a second range of quantizer levels during normal operation, wherein more quantizer levels are in said first range than in said second range.

6. The method of Claim 1, wherein said enabling step enables at least two additional quantizer levels at a low end of a quantizer range.

7. The method of Claim 6, wherein:

the range of quantizer levels for normal operation of the modulator is from –6 to +6; and

the range of quantizer levels for ramp up operation of the modulator is from –8 to +7.

8. A variable-level quantizer, comprising:

an input for receiving a value from a summer;

a truncation circuit which provides a quantized value based on a plurality of most significant bits of the summer value; and

a clipping circuit which selectively adjusts the quantized value within a first range of quantizer levels during a ramp up sequence and within a second range of quantizer levels during normal operation, wherein more quantizer levels are in said first range than in said second range.

9. The variable-level quantizer of Claim 8, further comprising an output connected to said clipping circuit, said output being adapted for interconnection to an input of a pulse-width modulation encoder.

10. The variable-level quantizer of Claim 8, wherein:

said input is adapted to receive a 12-bit summer value; and

said truncation circuit provides a 4-bit quantized value.

11. The variable-level quantizer of Claim 8, wherein said first range of quantizer levels enables at least two additional quantizer levels from a low end of said second range.

12. The variable-level quantizer of Claim 11, wherein:

the first range of quantizer levels for ramp up operation is from –8 to +7; and

the second range of quantizer levels for normal operation is from –6 to +6.

13. A delta-sigma modulator comprising:

an input;

a plurality of integrators connected to said input, said integrators having respective outputs;

a summer which adds a selection of the integrator outputs and the input to yield a summer output; and

a quantizer which quantizes the summer output, said quantizer selectively enabling an additional quantizer level during a ramp up sequence of the modulator.

14. The delta-sigma modulator of Claim 13, wherein the additional quantizer level is disabled during normal operation of the modulator.

15. The delta-sigma modulator of Claim 13, wherein said quantizer truncates the summer output.

16. The delta-sigma modulator of Claim 13, wherein said quantizer further clips a truncated sum within a first range of quantizer levels during the ramp up sequence and within a second range of quantizer levels during normal operation, wherein more quantizer levels are in said first range than in said second range.

17. The delta-sigma modulator of Claim 16, wherein said first range of quantizer levels enables at least two additional quantizer levels from a low end of said second range.

18. The delta-sigma modulator of Claim 17, wherein:

the first range of quantizer levels for ramp up operation is from –8 to +7; and

the second range of quantizer levels for normal operation is from –6 to +6.

19. A digital-to-analog converter, comprising:

an input for receiving a digital signal;

a delta-sigma modulator connected to said input, said delta-sigma modulator using a variable-level quantizer which selectively enables an additional quantizer level during a ramp up sequence of the modulator; and

a pulse-width modulation encoder which generates a pulse-modulated signal based on an output from said variable-level quantizer.

20. The digital-to-analog converter of Claim 19, further comprising a low-pass filter connected to said pulse-width modulation encoder.

21. The digital-to-analog converter of Claim 19, wherein said variable-level quantizer selectively enables at least two additional quantizer levels at a low end of a quantizer range.

22. The digital-to-analog converter of Claim 19, wherein said variable-level quantizer provides a 4-bit quantized value.